ARQUIMEA

ARQ_17501_DSP_003 v03

17501 LVDS

AQLVR02 RECEIVER4X DETAILED SPECIFICATION

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Notice

CHANGE CONTROL

ISSUE	DATE	SECTION	DESCRIPTION
01	15/12/2017	All	Initial Release
02	31/01/2018	All p12	Correction of Minor bugs on the part-type Update of marking requirement
03	05/10/2021	p 7, 11, 12, Chapter 4 & 5.3	Update of marking requirement, update package drawing, update electrical parameters. Change of format.

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1. Introduction

1.1. Scope

This specification details the ratings, physical and electrical characteristics, test and inspection data for the component type variants and/or the range of components specified herein. It complements the requirements of RD-1, and shall be read in conjunction with the ESCC Generic Specification listed under Applicable Documents

1.2. Documents

1.2.1. Applicable documents

Ref.	Number	Title
[AD-1]	ECSS-Q-ST-60C	Space product Assurance for EEE parts
[AD-2]	ECSS-Q-ST-60-02C	ASIC and FPGA development, 31 July 2008
[AD-3]	ESCC9000	Monolithic, Hermetically sealed IC Generic Specification
[AD-4]	MIL-STD-883	Test Methods and Procedures for Microelectronics.

Table 1.1 List of Applicable Documents

1.2.2. Reference documents

Ref.	Number	Title
[RD-2]	ARQ_15601_DSH_003	LVDS Quad Receiver AQLVR02 Datasheet

Table 1.2 List of Reference Documents

1.3. Acronyms and abbreviations

AD	Applicable Document(s)
ASIC	Application Specific Integrated Circuit
ff	fast-fast
FPGA	Field Programmable Gate Array
IC	Integrated Circuit
ICM	Input Common Mode
LVDS	Low Voltage Differential Signaling
RD	Reference Document(s)
ss	slow-slow
TBC	To Be Confirmed
tf	Fall Time
TID	Total Ionizing Dose
tr	Rise Time
tt	typical-typical
UI	Unit Interval time
VCM	Common Mode Voltage
VHDL	Hardware Description Language
VHSIC	Very High Speed Integrated Circuit
VID	Differential Input Voltage
VIH	High Level Input Voltage
VIL	Low Level Input Voltage
VOD	Differential Output Voltage

2. Part type and type variant

2.1.1. Part Type

The Part type is AQLVR02S2

- AQLVR02: Component Reference
- S: Space Quality Level according to ESCC9000
  - SEL>60MeV/mg/cm2
  - BER<10-13 BER/day
  - TID>300krad
- Variant 01: FP-16 Ceramic Dual Flat Pack

2.1.2. Type Variant

Part Type ordering number	Quality level	Package	Operating Temperature	Terminal material and finish (*)
AQLVR02.E2	Standard	FP-16	-55ºC to 125ºC	D2
AQLVR02.S2	ESCC9000	FP-16	-55ºC to 125ºC	D2

Table 2.1: Variant Type

(*) The terminal material and/or finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500

2.2. Maximum ratings

The maximum ratings of the technology used for AQLVR02, which shall not be exceeded at any time during use or storage, are as presented in table below:

Symbol	Parameter	Value
V_{DD}	DC supply voltage	-0.5 to 4.6V
V_I	TTL/CMOS Input Voltage	-0.5V to 6V
V_{IN}	LVDS Input Voltage	-5V to 6V
T_{STG}	Storage temperature	-65ºC to +150ºC
T_J	Maximum junction temperature	+175ºC
Tc	Maximum Case temperature	+125ºC
ESD	ESD Last Passing Voltage – HBM	8kV
P_D	Power dissipation	850mW

Table 2.2: Absolute Maximum Rating

Note:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
2. The Recommended Operating as well as derated Conditions according to ECSS-Q-30-11A are presented below:

Symbol	Parameter	Operating Value	Derated Value
V_{DD}	Power supply voltage	3.0 to 3.6V	3.0 to 3.6V
V_{IN}	TTL/CMOS Input Voltage	0 to 5V	0 to 5V
	LVDS Input Voltage, receiver inputs	-4.6V to 5.6V	-4.6V to 5.6V
V_{CM}	LVDS Input Common Mode Voltage	-4V to 5V	-4V to 5V
T_C	Case temperature range	-55ºC to +125 ^{O}C	+100ºC (Tj=110ºC)

Table 2.3: Recommended Operating Conditions

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

3. **Handling precautions**

The component could be susceptible to damages by electro-static discharge. Therefore, suitable precautions shall be taken for protection during all phases of manufacture, testing, packaging, shipment and any additional handling. The following guidelines are applicable:

- Always manipulate the devices in an ESD controlled environment.
- Always store the devices in a shielded environment that protects against ESD damage (at least a non-ESD generating tray and a metal bag).
- Always wear a wrist strap when handling the devices and use ESD safe gloves.

These components are categorized as Class 2 per ESCC Basic Specification No. 23800 with Minimum Critical Path Failure Voltage of:

- HBM: ≥ 2kV
- CDM: ≥ +/- 500V

4. Physical dimensions and terminal identification

Consolidated Notes are given following the case drawings and dimensions

4.1.1. FP-16

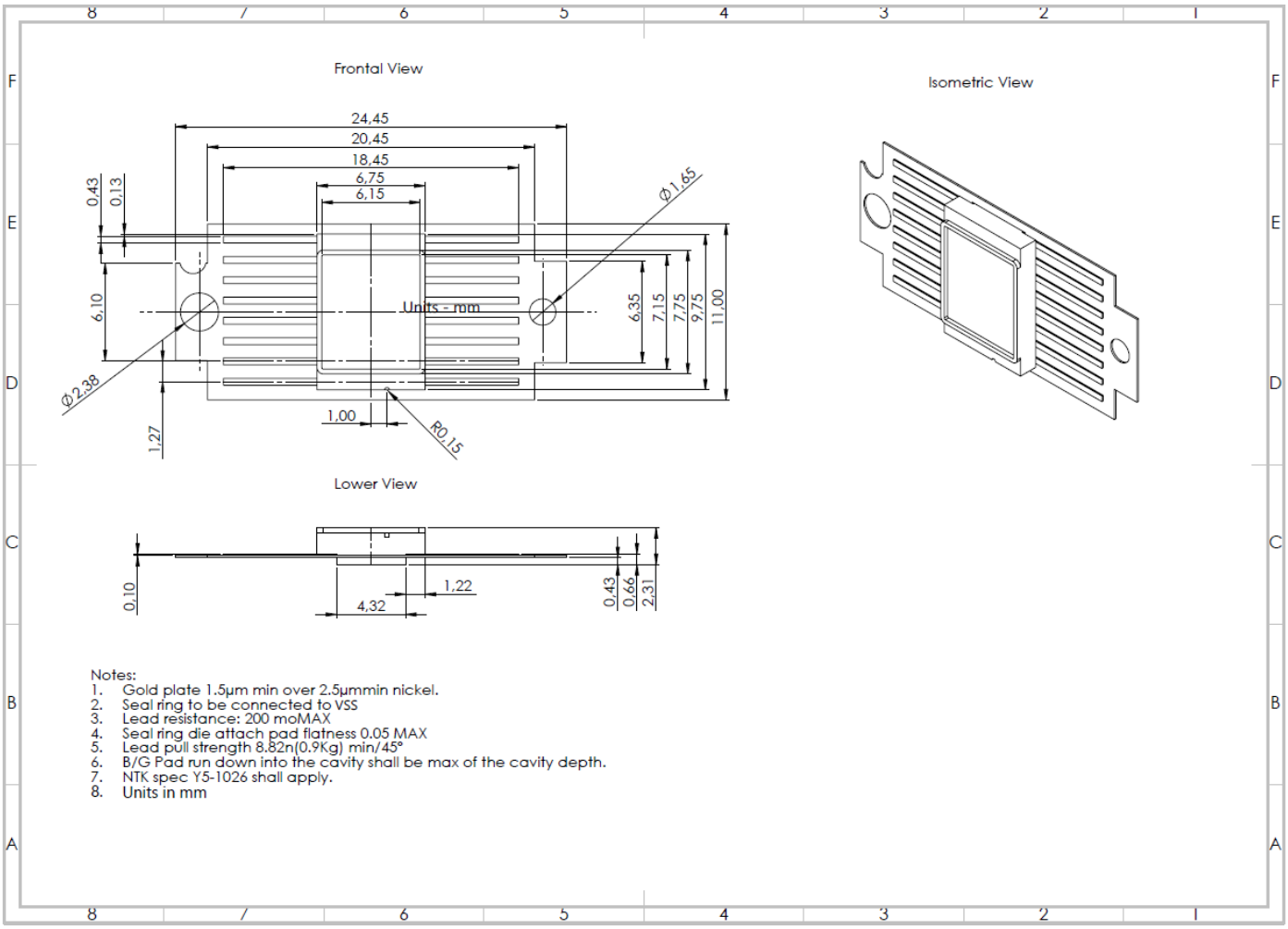


Figure 4.1: Package Drawing

4.1.2. Notes to Physical Dimensions and Terminal Identification

Notes to Physical Dimensions and Terminal Identification

1. An Index mark shall be located adjacent to Pin 1.
2. The dimension shall be measured from the seating plane to the base plane.
3. The true position pin spacing is 1.27mm between centrelines. Each pin centreline shall be located within ±0.13mm of its true longitudinal position relative to Pin 1 and the highest pin number

4.2. Functional diagram

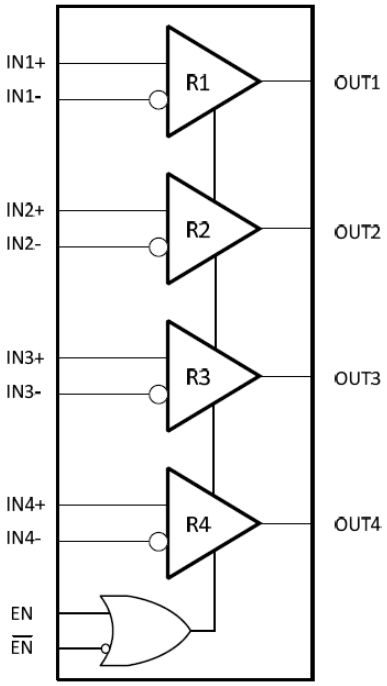


Figure 4.2: Block Diagram

4.3. Pin Assignment

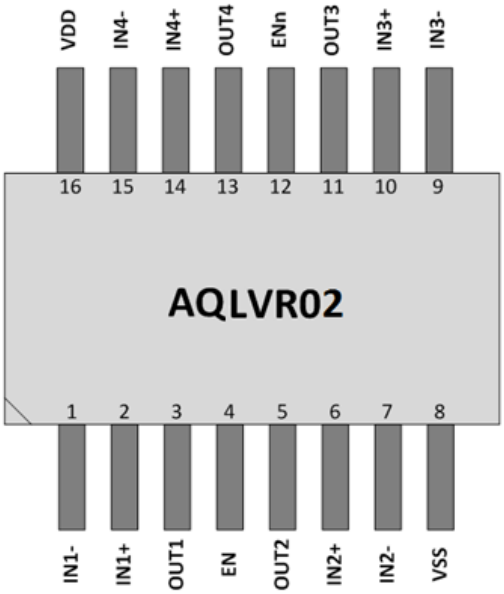


Figure 4.3: Pinout Diagram

Pin Nº	Name	Type	Description
1	IN1-	LVDS Input	Inverting LVDS input, channel 1
2	IN1+	LVDS Input	Non-Inverting LVDS input, channel 1
3	OUT1	Digital Output	CMOS/TTL output, channel 1
4	EN	Digital Input	Logic enable for the LVDS receivers

Pin Nº	Name	Type	Description
5	OUT2	Digital Output	CMOS/TTL output, channel 2
6	IN2+	LVDS Input	Non-Inverting LVDS input, channel 2
7	IN2-	LVDS Input	Inverting LVDS input, channel 2
8	VSS	Power	Ground
9	IN3-	LVDS Input	Inverting LVDS input, channel 3
10	IN3+	LVDS Input	Non-Inverting LVDS input, channel 3
11	OUT3	Digital Output	CMOS/TTL output, channel 3
12	ENn	Digital Input	Logic active low enable for the LVDS receivers
13	OUT4	Digital Output	CMOS/TTL output, channel 4
14	IN4+	LVDS Input	Non-Inverting LVDS input, channel 4
15	IN4-	LVDS Input	Inverting LVDS input, channel 4
16	VDD	Power	3.3 V Power

Table 4.1: Pinout Description

4.4. Storage

The components must be stored in a temperature, humidity and ESD controlled environment as per ECSS-24900. Specific storage conditions are:

- Normal air, relative humidity 55%±10%, temperature 17 to 27°C

Shelf life of 10 years as per relifing procedure ECSS-Q-ST-60-14.

5. Requirements

5.1. General

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.

5.1.1. Deviation from the generic specification

High Temperature Reverse Bias Burn-in shall not be performed. Not Applicable.

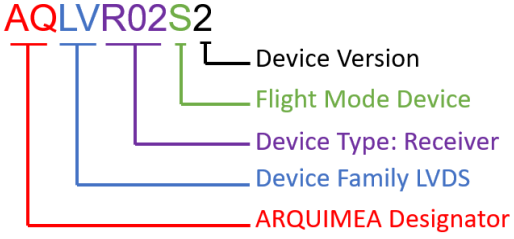
5.2. Marking

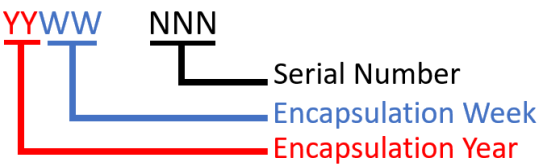
The marking is based on the requirements of ESCC Basic Specification No. 21700 and are identified as follows:

Figure 5-1: Marking Example

Where it has marked:

- ARQUIMEA's symbol
- The Entire Part-type (as per ARQ internal Nomenclature)
- Date Code: Four-digit code number shall be used for the manufacturing date. The first two digits shall be the last two figures of the year of manufacture. The last two digits shall indicate the week of the year which encapsulation or the final production process occurred.
- Serial Number: A serial number consisting of three digits shall be used. run sequentially and shall not duplicated.





5.3. Electrical measurements at room, high and low temperatures

Electrical measurements shall be performed at room, high and low temperatures. Consolidated notes are given after the tables.

5.3.1. Room Temperature Electrical Measurements

The measurements shall be performed at Tamb = +22 ±3 ºC.

Unless otherwise stated, these specifications apply for VDD = 3.3V±0.3V and VSS=GND

Symbol	Parameter	Condition (Note 1)	Min	Max	Unit
FUNCTIONAL TEST					
FT	Functional Test	See Note 6 V_{ID}=±200mV (400mVpp)			
TTL/CMOS DC SPECIFICATIONS (EN)					
V_{IH}	High-level input voltage		2.0	5V	V
V_{IL}	Low-level input voltage		-0.3	0.8	V
I_{IH}	High-level input current	V_{DD} = 3.6V, V_{IN} = 3.6V	-10	+10	µA
I_{IL}	Low-level input current	V_{DD} = 3.6V, V_{IN} = 0V	-10	+10	µA
I_{CS}	Cold Spare Leakage current	V_{DD} = V_{SS}, V_{IN} = 3.6V	-5	+5	µA
TTL/CMOS OUTPUT DC SPECIFICATIONS (OUT)					
V_{OH}	High-level output voltage	V_{DD} = 3.0V, I_{OH} = -0.4mA	2.2	V_{DD}	V
		V_{DD} = 3.0V, I_{OH} = -2mA	2.1	V_{DD}	V
		V_{DD} = 3.0V, I_{OH} = -4mA	2.0	V_{DD}	V
V_{OL}	Low-level output voltage	V_{DD} = 3.0V, I_{OL} = 0.4mA	-0.3	0.4	V
		V_{DD} = 3.0V, I_{OL} = 2mA	-0.3	0.4	V
		V_{DD} = 3.0V, I_{OL} = 4mA	-0.3	0.4	V
I_{CS}	Cold Spare Leakage current	V_{DD} = V_{SS}, V_{OUT} = 3.6 V	-5	+5	µA
I_{OZ}	Output Tri-State Current	V_{DD} = 3.6V, Tri-State output (channel disabled), V_{OUT} = V_{DD} or V_{SS}	-15	+15	µA
I_{OS}	Output Short Circuit Current (Note 5)	V_{DD} = 3.6V, High Level output, V_{OUT} = 0 V		-150	Ma
LVDS RECEIVER DC SPECIFICATIONS (IN+, IN-)					
V_{TH}	Differential Input High Threshold	V_{CMI} = -4V, +1,2V, +5V		+100	mV
V_{TL}	Differential Input Low Threshold	V_{CMI} = -4V, +1,2V, +5V	-100		mV
V_{ID_HYS}	Differential Input hysteresis	V_{TH} - V_{TL}	15		mV
V_{CMR}	Common Mode Voltage Range (Note 3)	V_{ID}=±200mV (400mVpp)	-4	+5	V

Symbol	Parameter	Condition (Note 1)	Min	Max	Unit
I_{IN}	LVDS Input Current	V_{DD} = +3.6V, V_{CMI} = +1.2V, V_{ID}=±400mV	-10	+10	µA
		V_{DD} = +3.6V, V_{CMI} = -4V to +5V, V_{IN+}=V_{IN-}=V_{CMI}	-20	+20	µA
ΔI_{IN}	Input Current Balance (I_{IN+}-I_{IN-})	V_{DD} = +3.6V, V_{CMI} = -4V to +5V, V_{IN+}=V_{IN-}=V_{CMI}	-6	+6	µA
I_{CSIN}	Cold Sparing Leakage Current	V_{DD} = V_{SS}, V_{CMI} = +1.2V, V_{ID}=±400mV	-10	+10	µA
		V_{DD} = V_{SS}, V_{CMI} = -4V to +5V, V_{IN+}=V_{IN-}=V_{CMI}	-20	+20	µA
C_{IN}	Input Capacitance	Note 2		3	pF
SUPPLY CURRENT					
I_{CLLS}	Total Static Supply Current	ENn = V_{SS}, EN = V_{DD}, V_{DD} = 3.6 V, Fq = DC, no load		60	mA
I_{CCZ}	Tri-State Supply Current	END, ENR = V_{SS}, V_{DD} = 3.6V, no load		10 (TBC)	mA
PSRR	Power Supply Rejection Ratio (Note 4)	R_L=100Ω, END=V_{DD}, V_{DD}=3.6V, Fq=250MHz, Power supply Fq=1MHz		-50	dB

Symbol	Parameter	Condition (Note 1)	Min	Max	Unit
t_{PHZ}	Disable Time (Active to Tri-State) High to Z	C_L = 10 pf		10	ns
t_{PLZ}	Disable Time (Active to Tri-State) Low to Z	C_L = 10 pf		10	ns
t_{PZH}	Enable Time (Tri-State to Active) Z to High	C_L = 10 pf		150	ns
t_{PZL}	Enable Time (Tri-State to Active) Z to Low	C_L = 10 pf		150	ns
t_{LHT}	Rise Time, 20% to 80%	C_L = 10pf		1200	ps
t_{HLT}	Fall Time, 80% to 20%	C_L = 10pf		1200	ps
t_{PLHD}	Propagation Low to High Delay	C_L = 10 pf		4.5	ns
T_{PHLD}	Propagation High to Low Delay	C_L = 10 pf		4.5	ns
T_{SKEW}	Differential Skew	T_{PHLD} - T_{PLHD}		300	ps
T_{CCS}	Output Channel-to-Channel Skew			500	ps
T_{DDS}	Output Device-to-Device Skew			750	ps
t_{PJ}	Periodic Jitter	V_{ID}=±200mV (400mVpp), 50% duty cycle at 250MHz,		15	ps

Symbol	Parameter	Condition (Note 1)	Min	Max	Unit
		trise≤ 1ns (20% - 80%)			
t_{CCJ}	Cycle to Cycle Jitter	V_{ID}=±200mV (400mVpp), 50% duty cycle at 250MHz, trise≤ 1ns (20% - 80%)		40	ps
t_{PPJ}	Peak to Peak Jitter	V_{ID} = 2^(7)-1 PRBS pattern at 500Mbps, trise ≤ 1ns (20% - 80%)		250	ps
t_{DJ}	Deterministic Jitter	V_{ID} = 2^(7)-1 PRBS pattern at 500Mbps, trise ≤ 1ns (20% - 80%)		200	ps

Table 5.1: Room Electrical Measurements

5.3.2. High and Low Temperatures Electrical Measurements

The measurements shall be performed at Tamb=+125 (+0 -5)ºC & Tamb=-55 (+5 -0)ºC

Symbol	Parameter	Condition (Note 1)	Min	Max	Unit
The measured parameters, drifts and absolute limits are identical to the one presented in Table 5.1 and Table 5.3					

Table 5.2: High and Low Temperature Electrical Measurements

5.3.3. Notes to Electrical Measurement Tables

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic. Maximum Operation frequency is recommended.
   a. Digital Inputs not under test shall be connected to VSS or VDD
   b. Digital outputs not under test shall be open.
   c. Differential LVDS inputs not under test could be shorted or open with VCMI=1,2V
   d. Differential LVDS outputs not under test shall be loaded with 100 Ohm resistor
2. Guaranteed but not tested.
3. Measurements shall be performed as a go-no-go test on a 100% basis.
4. Read and record measurements shall be performed on a sample of 5 components
5. Only one output should be shorted at a time
6. Verify the functionality of the devices including Enable and Fail-safe modes

Symbol	Parameter	Condition (Note 1)	Min	Max	Unit
V_{FSH}	Differential Input Fail-Safe High Threshold	V_{CMI} = -4V, +1.2V, +5V, Hold time>500ns	+10		mV
V_{FSL}	Differential Input Fail-Safe Low Threshold	V_{CM} = -4V, +1.2V, +5V, Hold time>500ns		-10	mV
V_{ID_FS}	Differential Input Fail-safe Range	V_{FSH} - V_{FSL}	20		mV

5.4. Parameters drift values

Unless otherwise specified, the measurements shall be performed at Tamb = +22 ±3ºC.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Symbol	Parameter	Drift Value (Δ) LIMIT	Unit
TTL/CMOS DC SPECIFICATIONS (EN)			
V_{IH}	High-level input voltage	±0,02	V
V_{IL}	Low-level input voltage	±0,02	V
I_{IH}	High-level input current	±2	µA
I_{IL}	Low-level input current	±2	µA
I_{CS}	Cold Spare Leakage current	±1	µA
TTL/CMOS OUTPUT DC SPECIFICATIONS (OUT)			
V_{OH}	High-level output voltage	±0,02	V
V_{OL}	Low-level output voltage	±0,02	V
I_{CS}	Cold Spare Leakage current	±1	µA
I_{OZ}	Output Tri-State Current	±4	µA
I_{Os}	Output Short Circuit Current (Note 5)	±10	mA
LVDS RECEIVER DC SPECIFICATIONS (IN+, IN-)			
V_{TH}	Differential Input High Threshold	±20	mV
V_{TL}	Differential Input Low Threshold	±20	mV
V_{ID_HYS}	Differential Input hysteresis	±20	mV
V_{ID_FS}	Differential Input Fail-safe threshold	±20	mV
V_{CMR}	Common Mode Voltage Range	-	V
I_{IN}	Input Current	±2	µA
ΔI_{IN}	Input Current Balance (I_{IN+}-I_{IN-})	±1	uA
I_{CSIN}	Cold Sparing Leakage Current	±2	µA
SUPPLY CURRENT			
I_{CLLD}	Total Dynamic Supply Current	±10	mA
I_{CLLS}	Total Static Supply Current	±5	mA
I_{CCZ}	Tri-State Supply Current	±2	mA
t_{PHZ}	Disable Time (Active to Tri-State) High to Z	±1	ns
t_{PLZ}	Disable Time (Active to Tri-State) Low to Z	±1	ns
t_{PZH}	Enable Time (Tri-State to Active) Z to High	±25	ns
t_{PZL}	Enable Time (Tri-State to Active) Z to Low	±24	ns
t_{LHT}	Rise Time, 20% to 80%	±200	ps

Symbol	Parameter	Drift Value (Δ) LIMIT	Unit
t_{HLT}	Fall Time, 80% to 20%	±200	ps
t_{PLHD}	Propagation Low to High Delay	±2	ns
T_{PHLD}	Propagation High to Low Delay	±2	ns
T_{SKEW}	Differential Skew T_{PHLD} - T_{PLHD}	±50	ps
T_{CCS}	Output Channel-to-Channel Skew	±100	ps
T_{DDS}	Output Device-to-Device Skew	±150	ps
t_{PJ}	Periodic Jitter	±10	ps
t_{CCJ}	Cycle to Cycle Jitter	±10	ps
t_{PPJ}	Peak to Peak Jitter	±50	ps
t_{DJ}	Deterministic Jitter	±50	ps

Table 5.3: Parameters drift Values

5.5. Intermediate and end-point electrical measurements

Unless otherwise specified, the measurements shall be performed at Tamb = +22 ±3°C. The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic where specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Symbol	Parameter	Condition (Note 1)	Min	Max	Unit
The measured parameters, drifts and absolute limits are identical to the one presented in Table 5.3					

Table 5.4: Intermediate and End-point Electrical Measurements

NOTES:

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic.
2. The drift values (Δ) are applicable to the Operating Life test only.

5.6. High temperature reverse bias burn-in

The High Temperature reverse bias burn-In is not applicable for this device.

5.7. Power burn-in conditions

Characteristic	Symbol	Test Conditions	Unit
Ambient Temperature	Tamb	+125 (+0 -5)	ºC
Positive Supply Voltage	V_{DD}	3,6	V
Negative Supply Voltage	V_{SS}	0	V
Digital Inputs Voltage	V_{IN}	Vss/V_{DD}	V
LVDS Input Signal Frequency	Fcy	250	MHz
LVDS Differential Inputs Voltage Threshold IN+/IN-	V_T	Square signal ±350	mV
Digital Output Load	RL	10k (TBC)	Ohm

Table 5.5: Power Burn-In Conditions

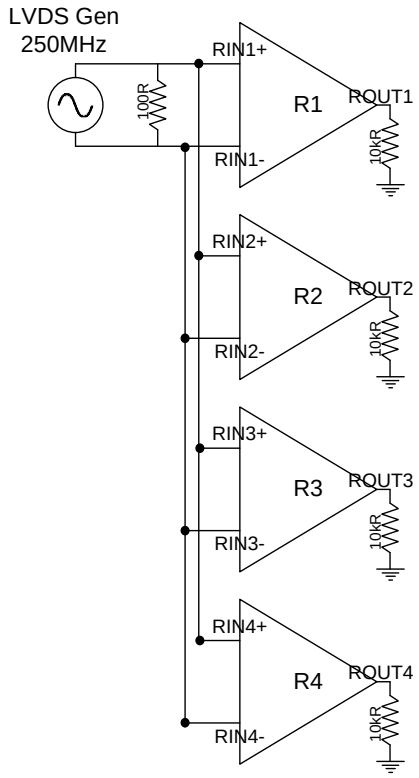


Figure 5.2: Power Burn-In Diagram

NOTES:

1. All Channels are connected to a single LVDS signal generator

5.8. Operating life conditions

The conditions shall be as specified for Power Burn-in.

5.9. Total dose radiation testing

5.9.1. Bias Conditions and Total Dose Level for Toral Dose Radiation Testing

Continuous bias shall be applied during irradiation testing as specified below.

The total dose level applied shall be as specified in the component type variant information herein or in the Purchase Order.

Characteristic	Symbol	Test Conditions	Unit
Ambient Temperature	Tamb	+22 (±3)	ºC
Positive Supply Voltage	V_{DD}	3,3	V
Negative Supply Voltage	V_{SS}	0	V
Digital Inputs Voltage	V_{IN}	Vss/V_{DD}	V
LVDS Input Signal Frequency	Fcy	DC 0	MHz
LVDS Differential Inputs Voltage Threshold IN+/IN-	V_T	DC +350	mV
Digital Output Load	RL	10k (TBC)	Ohm

Table 5.6: TID Conditions

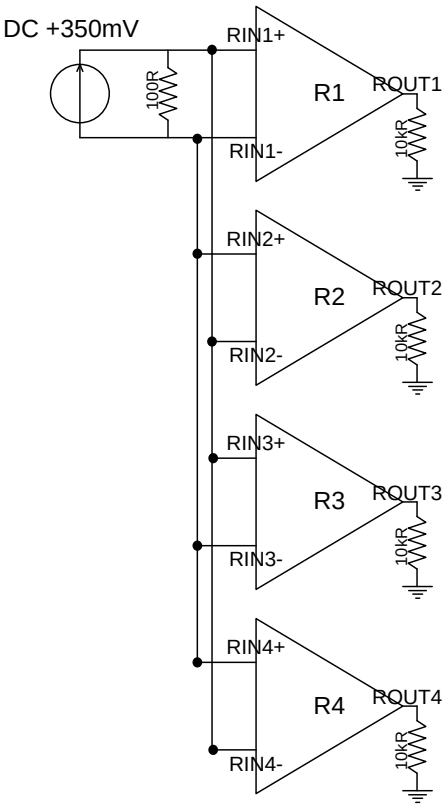


Figure 5.3: TID Diagram

NOTES:

1. All Channels are connected to a single source
2. Unbiased devices should have all pins connected to ground

5.9.2. Electrical Measurement for Total Dose Radiation Testing

Prior to irradiation testing the devices shall have successfully met Room Temperature Electrical Measurements specified herein.

Unless otherwise stated the measurements shall be performed at Tamb = +22 ±3°C.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The parameters to be measured during and on completion of irradiation testing are shown below.

Unless otherwise specified all inputs and outputs shall be tested for each characteristic.

Symbol	Parameter	Condition (Note 1)	Min	Max	Unit
The measured parameters, drifts and absolute limits are identical to the one presented in Table 5.3					

Table 5.7: Electrical Measurements for Total Dose Radiation Testing

6. Appendix: Agreed Deviations

Items affected	Description of Deviations
Deviations from Production test – Chart F2	None
Deviations from Screening Tests – Chart F3	None
Deviations from Qualification and Periodic Tests – Chart F4	None
Deviations from High and Low Temperatures Electrical Measurements	None
Deviations from Room Temperature Electrical Measurements	None